ADDI-DATA®
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Function Description

Incremental counter

APCIe-1711, CPCIs-1711, APCI-1710 and CPCI-1710
Multifunction counter board, optically isolated

DIN EN ISO 9001:2015 certified

Edition: 02.10-04/2022

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Warning!

The following risks result from the improper implementation of the board and from use contrary to the regulations:

Personal injury

Damage to the board, the PC and peripherals

Pollution of the environment.

- Protect yourself, others and the environment!
- Read the safety precautions (yellow leaflet) carefully!

  If this leaflet is not enclosed with the documentation, please contact us and ask for it.
- Observe the instructions of this manual!

  Make sure that you do not forget or skip any step!
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- Pay attention to the following symbols:

NOTICE!
Designates hints and other useful information.

NOTICE!
Designates a possibly dangerous situation.
If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed**.

WARNING!
Designates a possibly dangerous situation.
If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed** and persons may be **endangered**.

Contents

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Chapter overview

In this manual, you will find the following information:

Chapter	Content
1	Function description including block diagram and pin assignment
2	Standard software: Information on the API software functions
3	Appendix with index
4	Contact and support address

This document solely describes the function “Incremental counter”.

For general information on the **APCIe-/CPCIs-1711** or **APCI-/CPCI-1710**, please read the respective Technical Description of these boards (see PDF links). It contains, for example, the chapter “Inserting and installing the board” that supports you in commissioning.

1 Function description

The function “Incremental counter” is used to acquire signals shifted by 90°. To each function module, up to two incremental encoders can be connected.

Features:

- 4 function modules, each with 1 incremental counter (32-bit) or 2 incremental counters (16-bit)
- Processing of up to 5 MHz signals
- 4 programmable acquisition modes
- Single/double/quadruple analysis of 2 phase-shifted clock pulses (A, B)
- Detection of direction for upward or downward counting
- Hysteresis circuit to eliminate the first pulse after a change of rotational direction; can be switched off
- Two 32-bit data latches, individually programmable for internal/external strobe, latch strobe synchronised with internal clock
- Operating mode definition via internal mode register, loadable/readable through the data bus
- Strobe inputs which can be triggered either through 2 external pins (24 V input) or by writing in a register
- Interrupt display triggered through external strobe inputs
- Compare logic, index and reference point logic

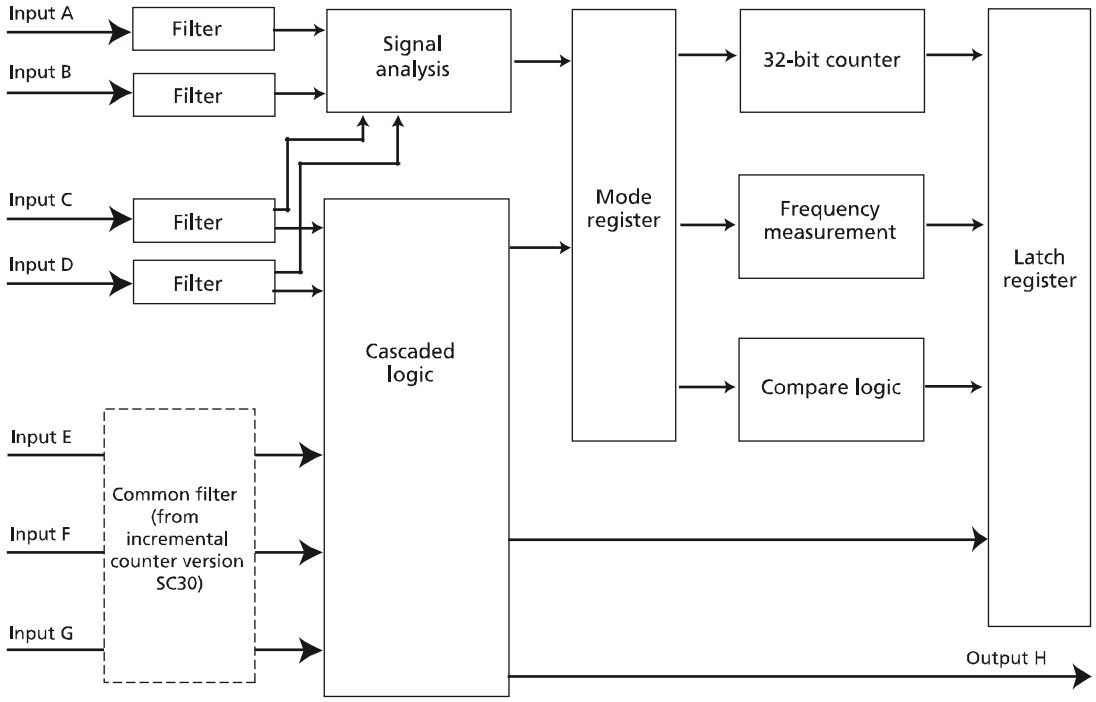
1.1 Board versions with “Incremental counter” function

NOTICE!
The “Incremental counter” function can be used with every version of the **APCIe-1711**, **CPCIs-1711, APCI-1710** or **CPCI-1710**.

The I/O specifications of the different board versions are available in the Technical Description of the **APCIe-/CPCIs-1711** or **APCI-/CPCI-1710** (see PDF links).

1.2 Block diagram

Fig. 1-1: Block diagram: “Incremental counter” function



1.3 Used signals

Table 1-1: Used signals

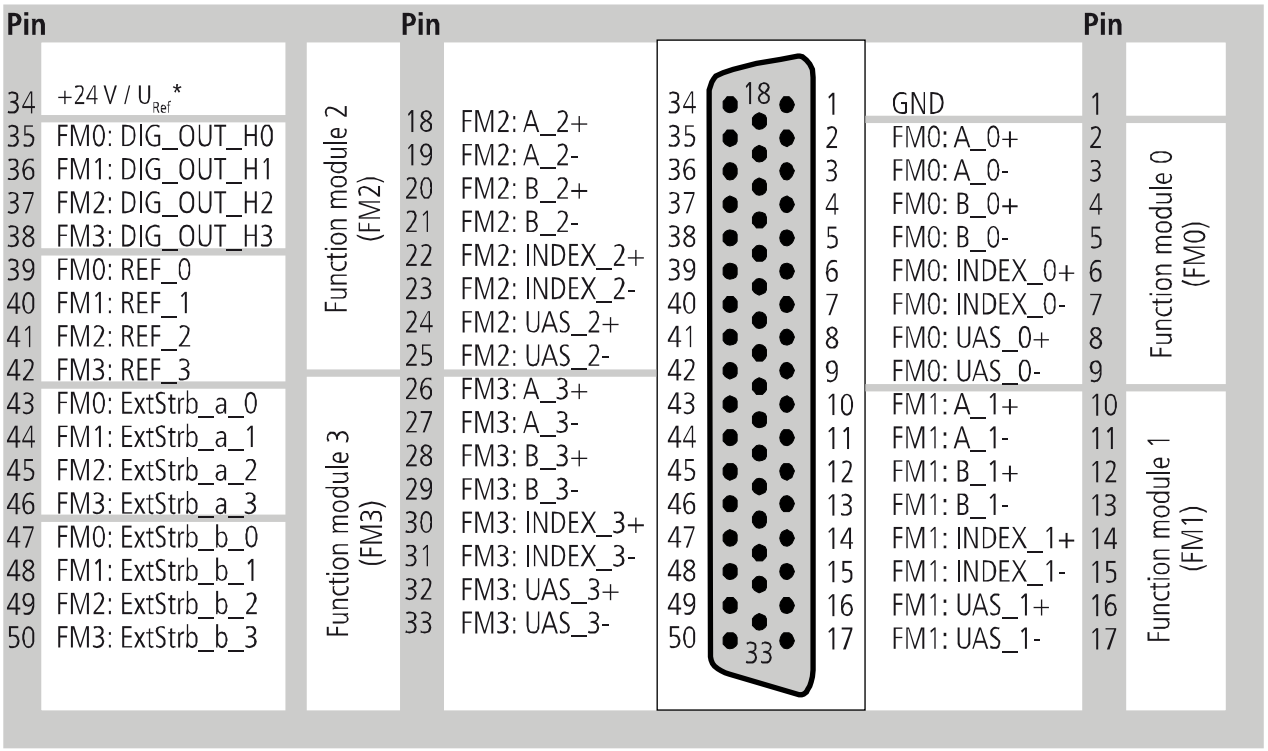
Signal name	Pin name	Signal type	Function
A_x+/-	Ax+/-	Differential/TTL/ 24 V*	Trace A of the incremental encoder (32-bit) or trace A of the incremental encoder 0 (16-bit)
B_x+/-	Bx+/-	Differential/TTL/ 24 V*	Trace B of the incremental encoder (32-bit) or trace B of the incremental encoder 0 (16-bit)
INDEX_x+/-	Cx+/-	Differential/TTL/ 24 V*	Index trace of the incremental encoder (32-bit)
C_x+/-			Trace A of the incremental encoder 1 (2 x 16-bit)
UAS_x+/-	Dx+/-	Differential/TTL/ 24 V*	Error signal input (32-bit)
D_x+/-			Trace B of the incremental encoder 1 (2 x 16-bit)
REF_x	Ex	24 V / optional 5 V	Digital input (can be used for the reference point logic)
ExtStrb_a_x	Fx	24 V / optional 5 V Active High	Digital input (can be used for the latch logic or interrupt logic)
ExtStrb_b_x	Gx	24 V / optional 5 V Active High	Digital input (can be used for the latch logic or interrupt logic)
DIG_OUT_Hx	Hx	24 V / optional 5 V	Digital output

x = Number of the function module (0-3)

* 24 V with 24 V board version

1.4 Pin assignment: Function modules

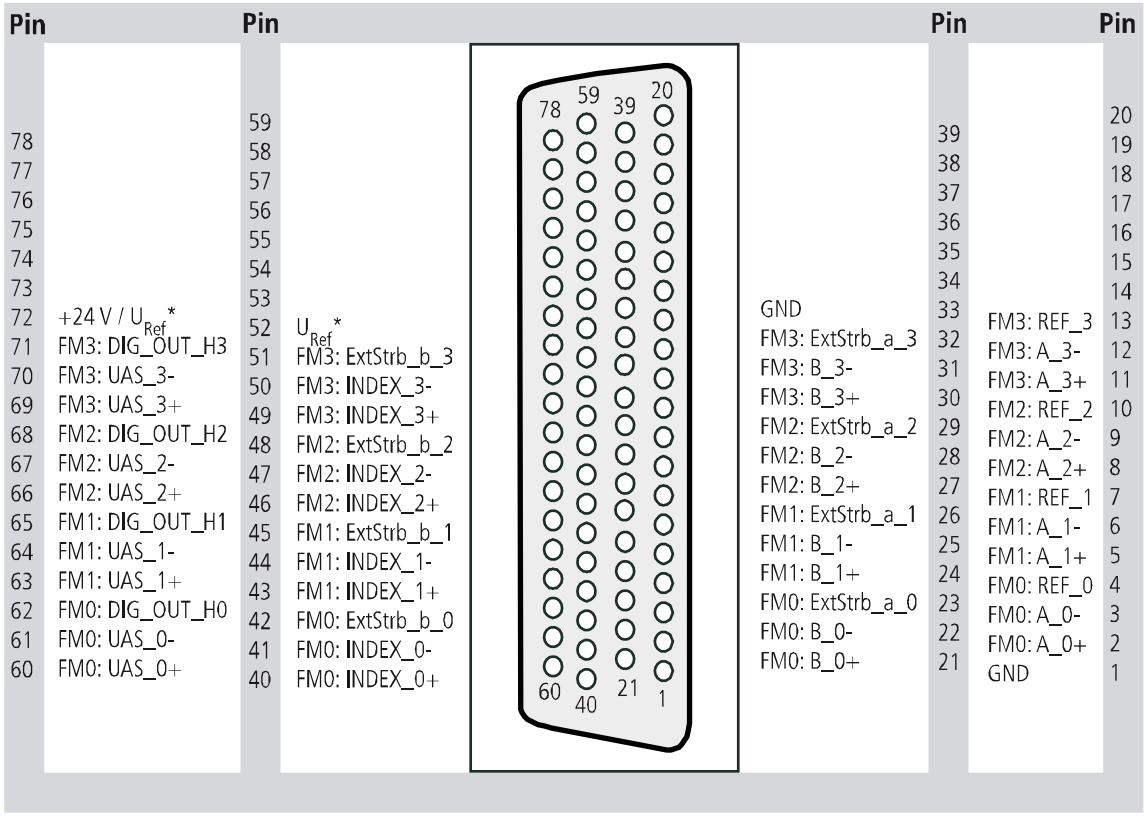
Fig. 1-2: Pin assignment: 50-pin D-Sub male connector (4 incremental counter modules)



* Pin 34: see Technical Description of the board

This pin assignment also applies to the **APCIe-1711** or **CPCIs-1711** if the cable **ST1711-50** is connected to the 78-pin D-Sub female connector of the board. For further information on this, please refer to the Technical Description of the **APCIe-1711** and **CPCIs-1711** (see PDF link).

Fig. 1-3: Pin assignment: 78-pin D-Sub female connector (APCIe-1711 and CPCIs-1711)



FM = Function module
* Pins 52 and 72: see Technical Description of the board

1.5 Connecting the incremental encoders

On the screw terminal panel **PX8001**, the pins of the 50 pin D-Sub female connector and the terminals connected to them are numbered in the same way. Thus, the terminal assignment of the screw terminal panel is identical with the pin assignment of the 50-pin D-Sub male connector of the **APCI-/CPCI-1710** or with that of the 50-pin D-Sub male connector on the **ST1711-50** cable **(APCIe-/CPCIs-1711)**.

The following table is to serve as a help for you when connecting the incremental encoders to the screw terminal panel. The blank fields in the “Incremental encoder” column can be filled in on the basis of the selected incremental encoder type.

Table 1-2: Connection of the incremental encoders to the screw terminal panel

Incremental encoder			Screw terminal panel PX8001 (50-pin)							
Pin No.	Pin name	Lead colour (cable)	Signal name	Terminal name	Signal type	Terminal No.				Terminal function
						FM0	FM1	FM2	FM3	
	+24 V / U_{Ref}		+24 V / U_{Ref}	+24 V / U_{Ref}	-	34	34	34	34	see Technical Description of the board
	GND		GND	GND	-	1	1	1	1	Ground
			A_x+	Ax+	Diff./TTL/24 V*	2	10	18	26	see Table 1-1
			A_x-	Ax-	Diff./TTL/24 V*	3	11	19	27	
			B_x+	Bx+	Diff./TTL/24 V*	4	12	20	28	see Table 1-1
			B_x-	Bx-	Diff./TTL/24 V*	5	13	21	29	
			INDEX_x+/- or C_x+/-	Cx+	Diff./TTL/24 V*	6	14	22	30	see Table 1-1
				Cx-	Diff./TTL/24 V*	7	15	23	31	
			UAS_x+/- or D_x+/-	Dx+	Diff./TTL/24 V*	8	16	24	32	see Table 1-1
				Dx-	Diff./TTL/24 V*	9	17	25	33	
			REF_x	Ex	24 V / opt. 5 V	39	40	41	42	see Table 1-1
			ExtStrb_a_x	Fx	see Table 1-1	43	44	45	46	see Table 1-1
			ExtStrb_b_x	Gx	see Table 1-1	47	48	49	50	see Table 1-1
			DIG_OUT_Hx	Hx	24 V / opt. 5 V	35	36	37	38	Digital output
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-

x = Number of the function module (0-3) * 24 V with 24 V board version

1.6 Acquisition modes

There are four modes available for the acquisition of incremental encoder signals.

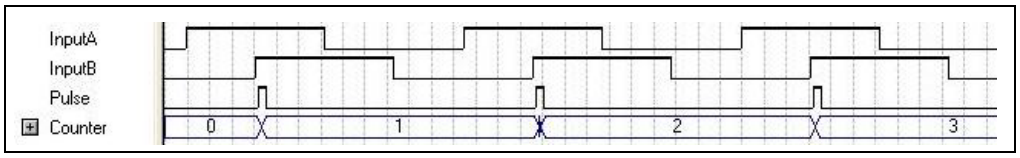
Table 1-3: Incremental counter: Acquisition modes

Mode	Feature
Single	Acquisition with a quarter of the highest possible resolution
Double	Acquisition with half of the highest possible resolution
Quadruple	Acquisition with the highest possible resolution
Direct	Acquisition without detection of the direction

a) Single mode

In single mode, if trace A of the incremental encoder signal is on “high”, the system counts with each rising edge of trace B.

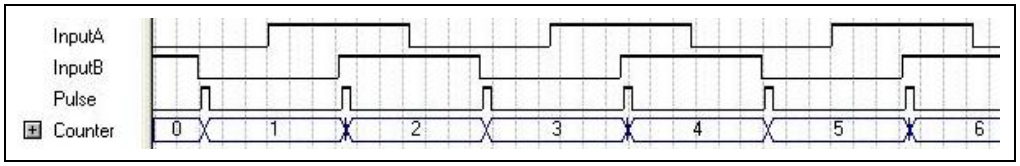
Fig. 1-4: Incremental counter: Single mode



b) Double mode

In double mode, the system counts with each rising and falling edge of trace B.

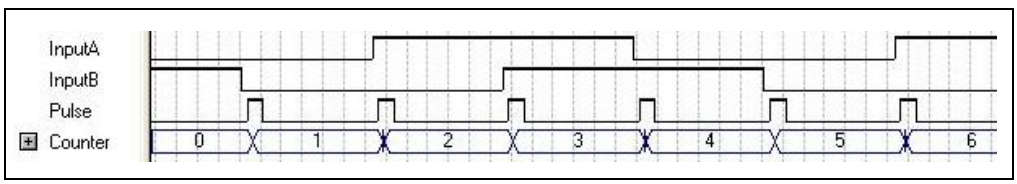
Fig. 1-5: Incremental counter: Double mode



c) Quadruple mode

In quadruple mode, the system counts with each rising and falling edge of traces A and B.

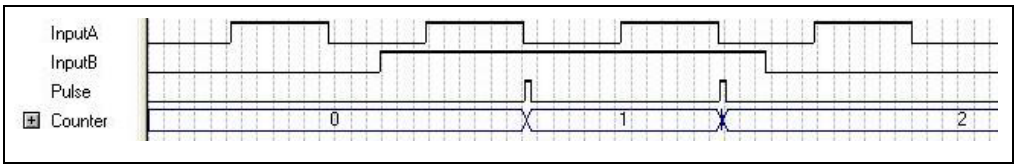
Fig. 1-6: Incremental counter: Quadruple mode



d) Direct mode

In direct mode, the system counts with each falling edge of trace A, with input B serving as a gate input. The system counts only if trace B is on “high”.
Moreover, in direct mode, the direction of counting can be programmed through software.

Fig. 1-7: Incremental counter: Direct mode

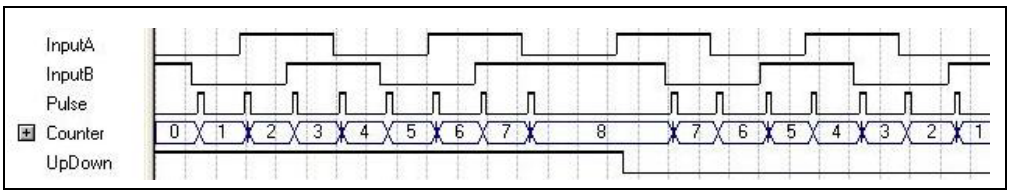


1.6.1 Options

1) Hysteresis function

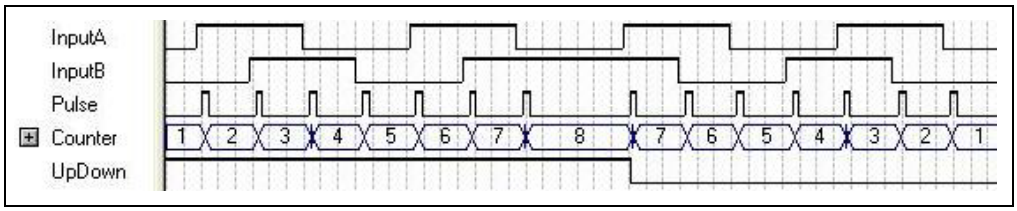
The hysteresis function can be used in single, double and quadruple mode.

Fig. 1-8: Quadruple mode: Hysteresis “on”



With hysteresis “on”, the first counting pulse after a change of rotational direction is not evaluated.

Fig. 1-9: Quadruple mode: Hysteresis “off”



2) Way of counting

In direct mode, counting can be either upwards or downwards.

1.7 Frequency measurement

During frequency measurement, all pulses within a selected time frame are counted.
This interval may take 200 ns to 6 ms. Depending on the mode set (see Chapter 1.6), a pulse is counted at a rising or falling edge of the incremental encoder signal.
The frequency measurement is started independently of the input signal through software. The 32-bit counter is set to zero then. When the measurement is finished, the frequency of the input signal is calculated from the length of the time frame and the number of counted pulses.

1.8 Compare logic

The compare logic mode has to be selected according to the incremental counter version:

a) Single Compare mode (up to incremental counter version SC27)

It is possible to use the compare logic in order to release an interrupt.
For this, a reference value (32-bit) needs to be indicated. As soon as the counter value corresponds to the reference value, an interrupt is released.

b) Modulo Compare mode (from incremental counter version SC30)

In this mode, an interrupt and/or at the digital output (Hx), a pulse of 400 µs can be released. The pulse is suited to trigger an external device such as a camera.
Like in Single Compare mode, also here a reference value (16-bit) needs to be indicated. When the counter value corresponds to the reference value (“ui_CompareValue”) or a multiple of it (including 0), the defined event is released. The same counter value releases another interrupt or pulse at the output only if it has deviated by the hysteresis value (8-bit) in the meantime (function: “i_PCIe1711_Init ModuloCompareLogic()” or “i_PCI1710_InitCompareLogic()”). This prevents the release of undesired interrupts with a sensor in rest position.

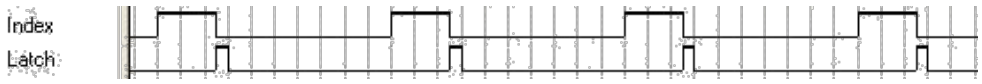
The release of the 400 µs pulse at the digital output (Hx) can be activated or deactivated via the software function “i_PCIe_1711_ConfigDigitalCHUse()” or “i_PCI1710_ConfigDigitalCHUse()”.
The function “i_PCI1710_ReadCompareLatchRegister()” or “i_PCIe_1711_ReadCompareLatchRegister()” allows the counter value that has released the event to be read back.

1.9 Index and reference point logic

The index signal of an incremental encoder can be used either for latching or latching and deleting the counter value.
You can select if the rising edge, the falling edge or both edges of the index signal should be counted. Depending on the mode, the counter value is latched only once or endlessly, i.e. after each defined edge.

Examples

a) Index logic with falling edge in continuous mode



b) Index logic with rising edge in continuous mode and reference point logic with falling edge

In addition to the index logic, the reference point logic can be activated.
In this case, the defined edge of the index signal is counted only after a falling edge of the external reference signal. Further relevant edges of the index signal are not taken into account until the next falling edge of the reference signal has been counted.

c) Index logic with falling edge in continuous mode and reference point logic with falling edge in Auto mode

If an external reference signal is used for the reference point logic, the Auto mode can be activated.
In this case, after a falling edge of the reference signal, every second edge of the defined index signal edge is counted.

1.10 Digital filter

For the incremental counter inputs A to D, a programmable digital filter can be used to eliminate interfering signals. For each of these inputs, the filter can be set individually.
The filter time depends on the board and the clock frequency (see the following table). If the filter is activated (function: “i_PCIe1711_SetInputFilter()” or “i_PCI1710_SetInputFilter()”), every positive or negative pulse lasting shorter than the defined filter time is suppressed.

Table 1-4: Filter times

	Filter time range (ns) with clock frequency		
Board	**30 MHz**	**33 MHz**	**40 MHz**
APCIe-1711	-	-	100 to 800
CPCIs-1711	-	-	100 to 800

Board	Filter time range (ns) with clock frequency		
	30 MHz	33 MHz	40 MHz
APCI-1710	133 to 1067	121 to 970	100 to 800
CPCI-1710	133 to 1067	121 to 970	100 to 800

From the incremental counter version SC30, also for the digital 24 V or 5 V inputs (Ex, Fx, Gx) a programmable digital filter can be used (function: “i_PCI1710_SetInputFilterEFG()” or “i_PCIe1711_SetInputFilterEFG()”). The filter time is equal for all of these inputs and can lie in the range between 100 ns and 800 ns.

1.11 Retrieving the status

The following status bits can be retrieved via software functions:

- Level of the error signal input (Dx)
- Level of the reference input (Ex)
- Direction of counting
- Counter overflow
- Index status
- Status of the latch registers.

2 Standard software

The API software functions supported by the board are listed in an HTML document. A description of how to access the respective file can be found in the document “Quick installation PC boards” (see PDF link), in the chapter “Standard software”.

3 Appendix

3.1 Index

4 Contact and support

Do you have any questions? Write or call us:

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