

Function Description

ETM

APCLe-1711, CPCIs-1711, APCI-1710 and CPCI-1710

Multifunction counter board, optically isolated



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Warning!

The following risks result from the improper implementation of the board and from use contrary to the regulations:



Personal injury



Damage to the board, the PC and peripherals



Pollution of the environment.

- Protect yourself, others and the environment!
- Read the safety precautions (yellow leaflet) carefully!
If this leaflet is not enclosed with the documentation, please contact us and ask for it.
- Observe the instructions of this manual!
Make sure that you do not forget or skip any step!
We are not liable for damages resulting from the wrong use of the board.
- Pay attention to the following symbols:



NOTICE!

Designates hints and other useful information.



NOTICE!

Designates a possibly dangerous situation.

If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed**.



WARNING!

Designates a possibly dangerous situation.

If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed** and persons may be **endangered**.

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Chapter overview

In this manual, you will find the following information:

Chapter	Content
1	Function description including block diagram and pin assignment
2	Standard software: Information on the API software functions
3	Appendix with index
4	Contact and support address

This document solely describes the function "ETM".

For general information on the **APCLe-/CPCIs-1711** or **APCI-/CPCI-1710**, please read the respective Technical Description of these boards (see PDF links). It contains, for example, the chapter "Inserting and installing the board" that supports you in commissioning.

1 Function description

The “ETM” (Edge Time Measurement) function is a timer interface which allows measuring the duration of a signal period, and simultaneously, the high- or low-level time of this period. The duty cycle can be computed by means of a software function (see Chapter 2).

A function module with the “ETM” function has

- 1 timer to create a time base
- 2 counters (0 and 1) to measure the period duration
- 2 counters (0 and 1) to measure the high- or low-level time
- 2 gate inputs (0 and 1).

Features:

- Optical isolation of the inputs and outputs through opto-couplers to prevent ground loops
- Interrupt status at the end of a period
- Processing of up to 5 MHz signals
- Inputs and outputs invertible through software
- Software gate possible; timer can be read back

1.1 Board versions with “ETM” function



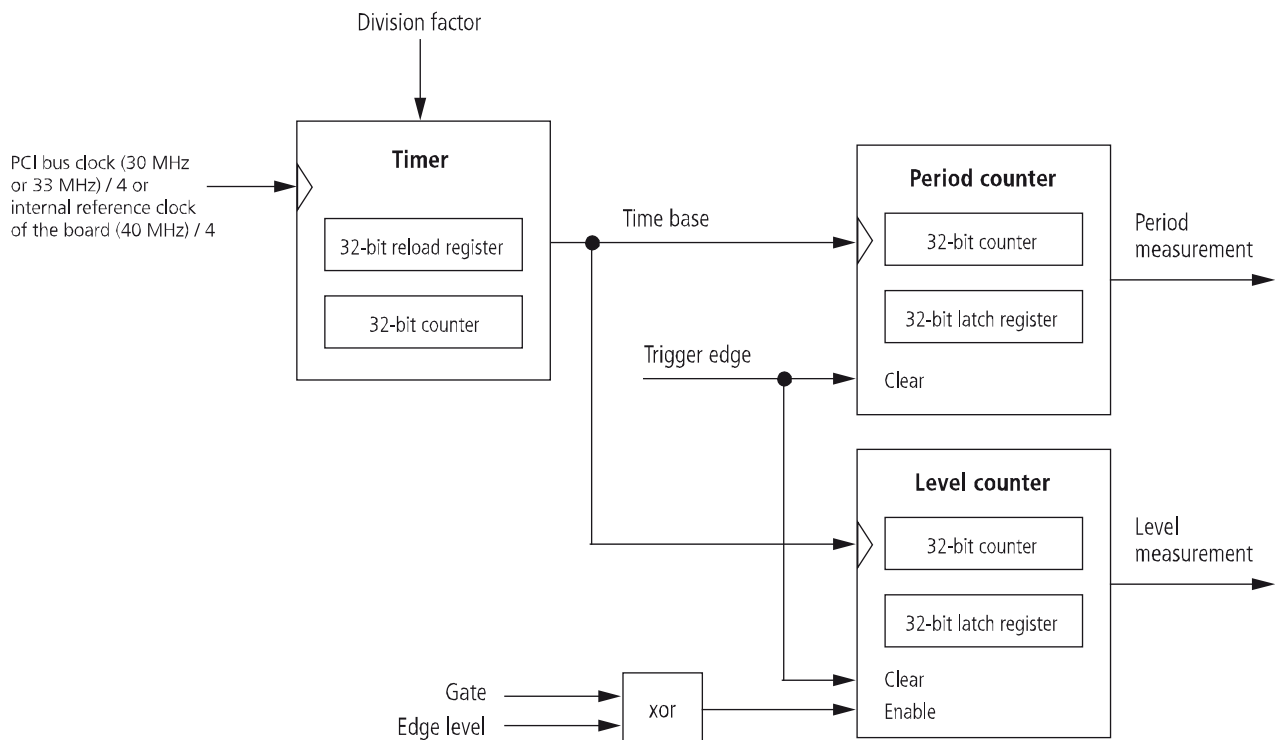
NOTICE!

The “ETM” function can be used with every version of the **APCLe-1711, CPCIs-1711, APCI-1710 or CPCI-1710**.

The I/O specifications of the different board versions are available in the Technical Description of the **APCLe-/CPCIs-1711** or **APCI-/CPCI-1710** (see PDF links).

1.2 Block diagram

Fig. 1-1: Block diagram: “ETM” function



1.3 Clock frequency

In addition to the internal reference clock, the PCI bus clock is available for compatibility reasons.



NOTICE!

As the PCI bus clock may vary strongly, it is recommended to use the internal reference clock.

Table 1-1: Clock frequencies

Board	PCI bus clock		Internal reference clock
	30 MHz	33 MHz	40 MHz
APCLe-1711	-	-	x
CPCIs-1711	-	-	x
APCI-1710	x	x	x
CPCI-1710	x	x	x

1.4 Used signals

On one board, you can operate a maximum of eight ETM, i.e. a maximum of two ETM per function module. With each function module, the "ETM" function uses four inputs (A to D).

Table 1-2: Used signals

Signal name	Pin name	Signal type	Function
Gate0_x+/-	Ax+/-	differential/TTL/ optional 24 V*	Gate input of ETM counter 0
Input0_x+/-	Bx+/-	differential/TTL/ optional 24 V*	Input of ETM counter 0
Gate1_x+/-	Cx+/-	differential/TTL/ optional 24 V*	Gate input of ETM counter 1
Input1_x+/-	Dx+/-	differential/TTL/ optional 24 V*	Input of ETM counter 1

x = Number of the function module (0-3)

* 24 V with 24 V board version

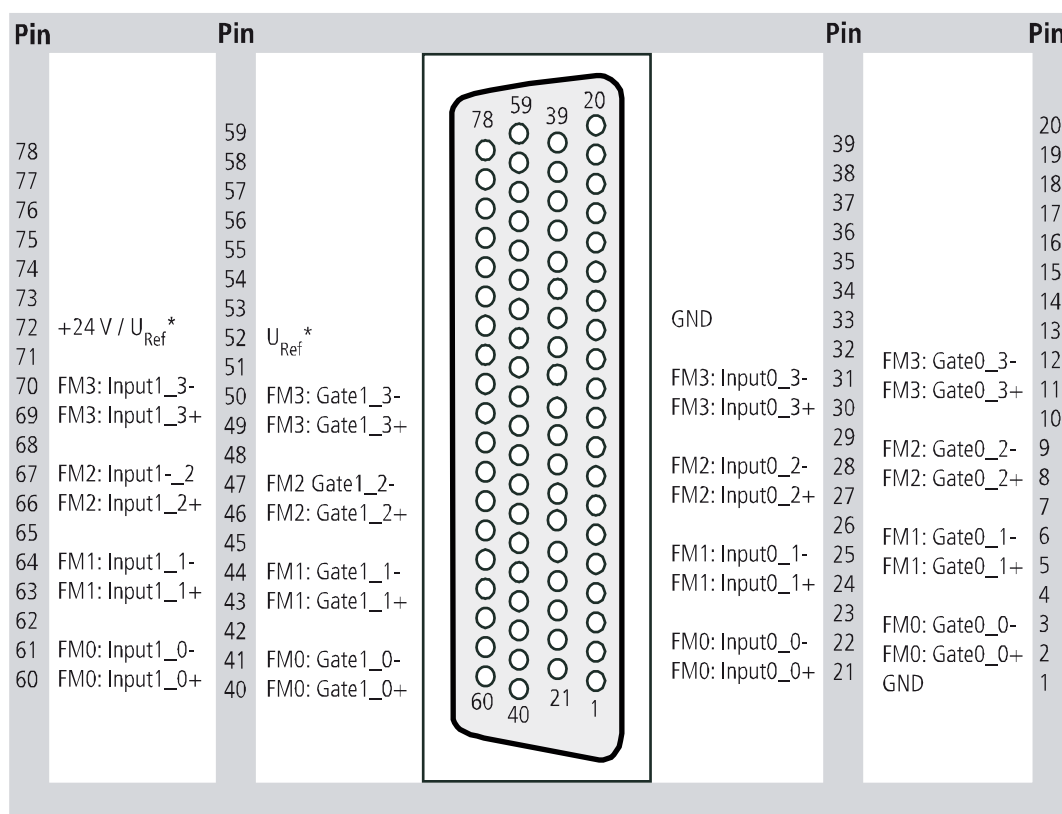
1.5 Pin assignment

Fig. 1-2: Pin assignment: 50-pin D-Sub male connector (4 ETM modules)

Pin		Pin				Pin			
34	+24 V / U _{Ref} [*]	18	FM2: Gate0_2+	34	18	1	GND	1	Function module 0 (FM0)
35		19	FM2: Gate0_2-	35		2	FM0: Gate0_0+	2	
36		20	FM2: Input0_2+	36		3	FM0: Gate0_0-	3	
37		21	FM2: Input0_2-	37		4	FM0: Input0_0+	4	
38		22	FM2: Gate1_2+	38		5	FM0: Input0_0-	5	
39		23	FM2: Gate1_2-	39		6	FM0: Gate1_0+	6	
40		24	FM2: Input1_2+	40		7	FM0: Gate1_0-	7	
41		25	FM2: Input1_2-	41		8	FM0: Input1_0+	8	
42		26	FM3: Gate0_3+	42		9	FM0: Input1_0-	9	
43		27	FM3: Gate0_3-	43		10	FM1: Gate0_1+	10	Function module 1 (FM1)
44		28	FM3: Input0_3+	44		11	FM1: Gate0_1-	11	
45		29	FM3: Input0_3-	45		12	FM1: Input0_1+	12	
46		30	FM3: Gate1_3+	46		13	FM1: Input0_1-	13	
47		31	FM3: Gate1_3-	47		14	FM1: Gate1_1+	14	
48		32	FM3: Input1_3+	48		15	FM1: Gate1_1-	15	
49		33	FM3: Input1_3-	49		16	FM1: Input1_1+	16	
50				50		17	FM1: Input1_1-	17	

* Pin 34: see Technical Description of the board

This pin assignment also applies to the **APC1e-1711** or **CPC1s-1711** if the cable **ST1711-50** is connected to the 78-pin D-Sub female connector of the board. For further information on this, please refer to the Technical Description of the **APC1e-1711** and **CPC1s-1711** (see PDF link).

Fig. 1-3: 78-pin D-Sub female connector (APC1e-1711 and CPC1s-1711)

FM = Function module

* Pins 52 and 72: see Technical Description of the board

1.6 Connecting the signal generators

1.6.1 Connection to the screw terminal panel

On the screw terminal panel **PX8001**, the pins of the 50 pin D-Sub female connector and the terminals connected to them are numbered in the same way. Thus, the terminal assignment of the screw terminal panel is identical with the pin assignment of the 50-pin D-Sub male connector of the **APCI-/CPCI-1710** or with that of the 50-pin D-Sub male connector on the **ST1711-50** cable (**APC1e-/CPC1s-1711**).

The following table is to serve as a help for you when connecting the signal generators to the screw terminal panel. The blank fields in the "Signal generator" column can be filled in on the basis of the selected signal generator type.

Table 1-3: Connection of the signal generators to the screw terminal panel

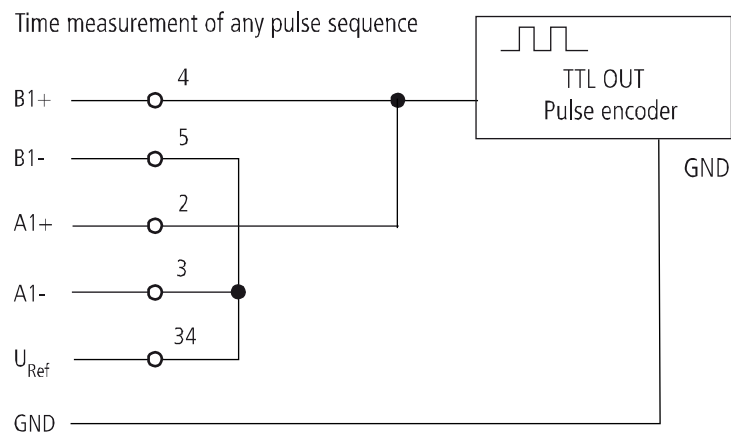
Signal generator			Screw terminal panel PX8001 (50-pin)							
Pin No.	Pin name	Lead colour (cable)	Signal name	Terminal name	Signal type	Terminal No.				Terminal function
						FM0	FM1	FM2	FM3	
	+24 V / U _{Ref}		+24 V / U _{Ref}	+24 V / U _{Ref}	-	34	34	34	34	see Technical Description of the board
	GND		GND	GND	-	1	1	1	1	Ground
			Gate0_x+	Ax+	Diff./TTL/ opt. 24 V*	2	10	18	26	Gate input of ETM counter 0
			Gate0_x-	Ax-		3	11	19	27	
			Input0_x+	Bx+	Diff./TTL/ opt. 24 V*	4	12	20	28	Input of ETM counter 0
			Input0_x-	Bx-		5	13	21	29	
			Gate1_x+	Cx+	Diff./TTL/ opt. 24 V*	6	14	22	30	Gate input of ETM counter 1
			Gate1_x-	Cx-		7	15	23	31	
			Input1_x+	Dx+	Diff./TTL/ opt. 24 V*	8	16	24	32	Input of ETM counter 1
			Input1_x-	Dx-		9	17	25	33	
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-

x = Number of the function module (0-3)

* 24 V with 24 V board version

1.7 Connection example

Fig. 1-4: Connection example



1.8 Functioning principle

Inputs B and D are used to release a trigger or an interrupt (see Fig. 1-6) and to measure the period duration.

If inputs A and C are set to "High" or "Low" (inverted mode), a counter increments with each clock cycle. The high- or low-level time is measured through these two inputs, too.

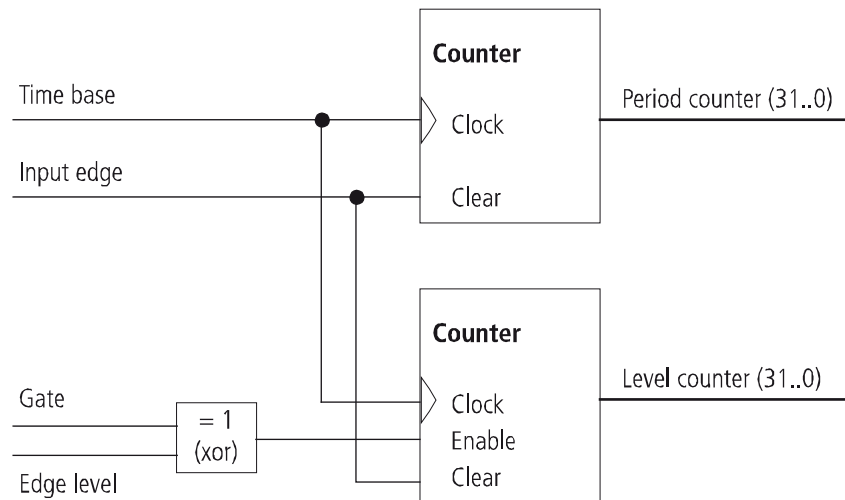
To carry out measurements, the respective signals have to be connected to the following inputs:

Table 1-4: Connection of the signals

Measurement	Input A	Input B	Input C	Input D
Period duration		x		x
Level time*	x	x	x	x
Duty cycle*	x	x	x	x

* Inputs A and B or C and D

Fig. 1-5: ETM counters



- **Time base:**

- Time value: PCI bus clock (**APCI-/CPCI-1710**: 30 MHz or 33 MHz, software-selectable) divided by 4 or internal reference clock (**APCIe-/CPCIs-1711**: 40 MHz) divided by 4 (= 10 MHz \pm 100 ppm)

**NOTICE!**

As the PCI bus clock may vary strongly, it is recommended to use the internal reference clock.

- Time unit: ns, μ s, ms (software-selectable)

- **Input edge:** Input of the ETM counter
- **Gate:** Gate of the ETM counter
- **Edge level:** is defined in the software initialisation

Fig. 1-6: Modes for ETM signal measurement

1.9 Procedure for using the ETM function

In order to use the ETM function, the following steps need to be performed:

- Connect the signal generator to the board.
- Parameterise the API software functions (time base, signal level, Single or Continuous mode):
 1. Select a function module.
 2. Select a clock signal, time value and time unit.
 3. Call up "i_PCle1711_InitETM" or "i_PCI1710_InitETM".
 4. Select a channel.
 5. Select an edge level and trigger level.
 6. Select a cycle mode, first trigger mode and interrupt mode.
 7. Call up "i_PCle1711_EnableETM" or "i_PCI1710_EnableETM".
- Read out the time measurement counter via polling or interrupt.
- Convert the time using the function "i_PCI1710_ConvertETMValue".

From the value of the time measurement counter and the time base, the period duration and the level time can be computed.

2 Standard software

The API software functions supported by the board are listed in an HTML document. A description of how to access the respective file can be found in the document "Quick installation PC boards" (see PDF link), in the chapter "Standard software".

3 Appendix

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4 Contact and support

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