

Function Description

PWM

APCLe-1711, CPCIs-1711, APCI-1710 and CPCI-1710

Multifunction counter board, optically isolated



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Warning!

The following risks result from the improper implementation of the board and from use contrary to the regulations:



Personal injury



Damage to the board, the PC and peripherals



Pollution of the environment.

- Protect yourself, others and the environment!
- Read the safety precautions (yellow leaflet) carefully!
If this leaflet is not enclosed with the documentation, please contact us and ask for it.
- Observe the instructions of this manual!
Make sure that you do not forget or skip any step!
We are not liable for damages resulting from the wrong use of the board.
- Pay attention to the following symbols:



NOTICE!

Designates hints and other useful information.



NOTICE!

Designates a possibly dangerous situation.

If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed**.



WARNING!

Designates a possibly dangerous situation.

If the instructions are ignored, the board, the PC and/or peripherals may be **destroyed** and persons may be **endangered**.

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Chapter overview

In this manual, you will find the following information:

Chapter	Content
1	Function description including block diagram and pin assignment
2	Standard software: Information on the API software functions
3	Appendix with index
4	Contact and support address

This document solely describes the function "PWM".

For general information on the **APCLe-/CPCIs-1711** or **APCI-/CPCI-1710**, please read the respective Technical Description of these boards (see PDF links). It contains, for example, the chapter "Inserting and installing the board" that supports you in commissioning.

1 Function description

The function "PWM" is an interface for pulse width modulation. It generates a frequency with an adjustable timing of the low and high level.

This function provides the following:

- 32-bit frequency generator to set low and high levels
- 2 inputs for start or stop gate
- 2 outputs for frequency output.

Properties:

- Optical isolation of the inputs and outputs through opto-couplers to prevent ground loops
- Interrupt status at the end of a period
- Signals of up to 3.33 MHz can be output
- Start level selection
- Stop level selection
- Hardware gate
- Software gate

1.1 Board versions with "PWM" function



NOTICE!

With the 24 V version of the **APCLe-1711**, **CPCIs-1711** or **APCI-1710**, the "PWM" function can be used only to a limited extent.

Table 1-1: Board versions with "PWM" function

Board version	"PWM" function
APCLe-1711	x
APCLe-1711-24V	x*
APCLe-1711-5V-I	x
CPCIs-1711	x
CPCIs-1711-24V	x*
CPCIs-1711-5V-I	x
APCI-1710	x
APCI-1710-24V	x*
APCI-1710-5V-I	x

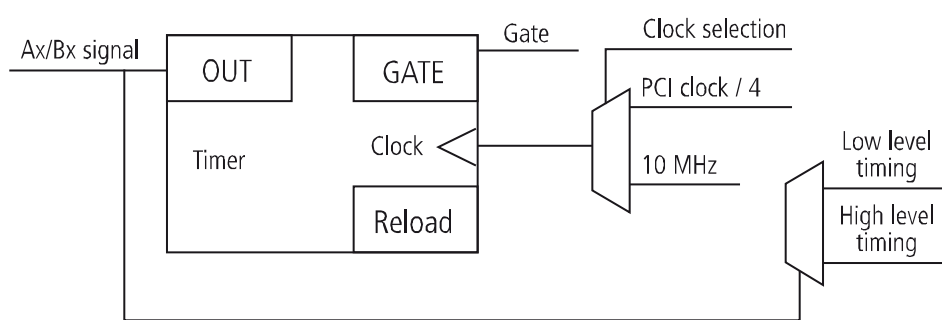
Board version	PWM function
APCI-1710-5V-I-O	x
CPCI-1710	x

* Only the 24 V digital output PWM0 (signal: DIG_OUT_H_x) is available. The maximum output frequency is load-dependent and limited by the 24 V output to 100 kHz (**APCIe-1711, CPCIs-1711**) or 5 kHz (**APCI-1710**).

The I/O specifications of the different board versions are available in the Technical Description of the **APCIe-/CPCIs-1711** or **APCI-/CPCI-1710** (see PDF links).

1.2 Block diagrams

Fig. 1-1: Block diagram: PWM function



1.3 Frequencies and level times

1.3.1 Clock frequency

The following clock frequencies are available:

Table 1-2: Clock frequencies

Board	Clock frequency		
	30 MHz	33 MHz	40 MHz
APCIe-1711	-	-	x
CPCIs-1711	-	-	x
APCI-1710	x	x	x
CPCI-1710	x	x	x

1.3.2 Minimal level time and maximum frequency



NOTICE!

Due to the hardware, the level time limits must not be under-run (see table below).

Table 1-3: Level time limits

Board	Output	Low level timing	High level timing	Max. output frequency
APCLe-/CPCIs-1711	Ax, Bx	150 ns	150 ns	3.33 MHz
	Hx	5 μ s	5 μ s	100 kHz
APCI-/CPCI-1710	Ax, Bx	250 ns	250 ns	2 MHz
	Hx	5 μ s	5 μ s	100 kHz

1.3.3 Level time calculation

Due to the clock and the structure of the PWM function, level times can be set only in certain steps. The requested level time is passed via software function when initialising PWM. The next shorter level time is automatically used and returned as a parameter for control.

The following actual level times for the low or high level are possible, but it has to be noted that the level times indicated in the table above must not be under-run:

Table 1-4: Level times

Level time (ns) with clock frequency		
30 MHz	33 MHz	40 MHz
200	181.8	150
333.3	303	250
466.7	424.2	350
600	545.5	450
733.3	666.7	550
866.7	787.9	650
100	909.1	750
⋮	⋮	⋮

Possible level times can be calculated as follows:

$$\text{Level time} = ((4 * x) + 6) * (1 / \text{clock frequency})$$

$$x = 0 \text{ to } 2^{32}-1$$

1.4 Used signals

With each function module, the PWM function uses three outputs (A, B and H) and five inputs (C to G).

Table 1-5: Used signals

Signal name	Pin name	Signal type	Function
PWM_OUT_Ch0_x+/-	Ax+/-	RS422/TTL output	PWM 0 output
PWM_OUT_Ch1_x+/-	Bx+/-	RS422/TTL output	PWM 1 output
GATE_Ch0_x+/-	Cx+/-	RS422/TTL input	PWM 0 gate input
GATE_Ch1_x+/-	Dx+/-	RS422/TTL input	PWM 1 gate input
DIG_IN_Ex	Ex	24 V input/optional 5V	Digital input
DIG_IN_Fx	Fx	24 V input/optional 5V	Digital input
DIG_IN_Gx	Gx	24 V input/optional 5V	Digital input
DIG_OUT_Hx	Hx	24 V output/optional 5V	Digital PWM 0 output or freely controllable

x = Number of the function module (0-3)

1.5 Pin assignment: Function modules

Fig. 1-2: Pin assignment: 50-pin D-Sub male connector (4 PWM modules)

Pin		Pin				Pin	
34	+24V / U _{Ref} *						
35	FM0: DIG_OUT_H0	18	FM2: OUT_Ch0_2+	34	18	1	GND
36	FM1: DIG_OUT_H1	19	FM2: OUT_Ch0_2-	35	19	2	FM0: OUT_Ch0_0+
37	FM2: DIG_OUT_H2	20	FM2: OUT_Ch1_2+	36	20	3	FM0: OUT_Ch0_0-
38	FM3: DIG_OUT_H3	21	FM2: OUT_Ch1_2-	37	21	4	FM0: OUT_Ch1_0+
39	FM0: DIG_IN_E0	22	FM2: GATE_Ch0_2+	38	22	5	FM0: OUT_Ch1_0-
40	FM1: DIG_IN_E1	23	FM2: GATE_Ch0_2-	39	23	6	FM0: GATE_Ch0_0+
41	FM2: DIG_IN_E2	24	FM2: GATE_Ch1_2+	40	24	7	FM0: GATE_Ch0_0-
42	FM3: DIG_IN_E3	25	FM2: GATE_Ch1_2-	41	25	8	FM0: GATE_Ch1_0+
43	FM0: DIG_IN_F0	26	FM3: OUT_Ch0_3+	42	26	9	FM0: GATE_Ch1_0-
44	FM1: DIG_IN_F1	27	FM3: OUT_Ch0_3-	43	27	10	FM1: OUT_Ch0_1+
45	FM2: DIG_IN_F2	28	FM3: OUT_Ch1_3+	44	28	11	FM1: OUT_Ch0_1-
46	FM3: DIG_IN_F3	29	FM3: OUT_Ch1_3-	45	29	12	FM1: OUT_Ch1_1+
47	FM0: DIG_IN_G0	30	FM3: GATE_Ch0_3+	46	30	13	FM1: OUT_Ch1_1-
48	FM1: DIG_IN_G1	31	FM3: GATE_Ch0_3-	47	31	14	FM1: GATE_Ch0_1+
49	FM2: DIG_IN_G2	32	FM3: GATE_Ch1_3+	48	32	15	FM1: GATE_Ch0_1-
50	FM3: DIG_IN_G3	33	FM3: GATE_Ch1_3-	49	33	16	FM1: GATE_Ch1_1+
				50	33	17	FM1: GATE_Ch1_1-

* Pin 34: see Technical Description of the board

This pin assignment also applies to the **APCLe-1711** or **CPCIs-1711** if the cable **ST1711-50** is connected to the 78-pin D-Sub female connector of the board. For further information on this, please refer to the Technical Description of the **APCLe-1711** and **CPCIs-1711** (see PDF link).

Fig. 1-3: Pin assignment: 78-pin D-Sub female connector (APC1e-1711 and CPC1s-1711)

Pin		Pin		Pin	Pin
78		59		39	20
77		58		38	19
76		57		37	18
75		56		36	17
74		55		35	16
73		54		34	15
72	+24 V / U _{Ref} *	53		33	14
71	FM3: DIG_OUT_H3	52	U _{Ref} *	32	FM3: DIG_IN_E3
70	FM3: GATE_Ch1_3-	51	FM3: DIG_IN_G3	31	FM3: OUT_Ch0_3-
69	FM3: GATE_Ch1_3+	50	FM3: GATE_Ch0_3-	30	FM3: OUT_Ch0_3+
68	FM2: DIG_OUT_H2	49	FM3: GATE_Ch0_3+	29	FM2: DIG_IN_E2
67	FM2: GATE_Ch1_2-	48	FM2: DIG_IN_G2	28	FM2: OUT_Ch0_2-
66	FM2: GATE_Ch1_2+	47	FM2: GATE_Ch0_2-	27	FM2: OUT_Ch0_2+
65	FM1: DIG_OUT_H1	46	FM2: GATE_Ch0_2+	26	FM1: DIG_IN_E1
64	FM1: GATE_Ch1_1-	45	FM1: DIG_IN_G1	25	FM1: OUT_Ch0_1-
63	FM1: GATE_Ch1_1+	44	FM1: GATE_Ch0_1-	24	FM1: OUT_Ch0_1+
62	FM0: DIG_OUT_H0	43	FM1: GATE_Ch0_1+	23	FM0: DIG_IN_E0
61	FM0: GATE_Ch1_0-	42	FM0: DIG_IN_G0	22	FM0: OUT_Ch0_0-
60	FM0: GATE_Ch1_0+	41	FM0: GATE_Ch0_0-	21	FM0: OUT_Ch0_0+
		40	FM0: GATE_Ch0_0+		GND

FM = Function module

* Pins 52 and 72: see Technical Description of the board

1.6 Connecting the signal generators

1.6.1 Connection to the screw terminal panel

On the screw terminal panel **PX8001**, the pins of the 50 pin D-Sub female connector and the terminals connected to them are numbered in the same way. Thus, the terminal assignment of the screw terminal panel is identical with the pin assignment of the 50-pin D-Sub male connector of the **APCI-/CPCI-1710** or with that of the 50-pin D-Sub male connector on the **ST1711-50** cable (**APC1e-/CPC1s-1711**).

The following table is to serve as a help for you when connecting the signal generators to the screw terminal panel. The blank fields in the "Signal generator" column can be filled in on the basis of the selected signal generator type.

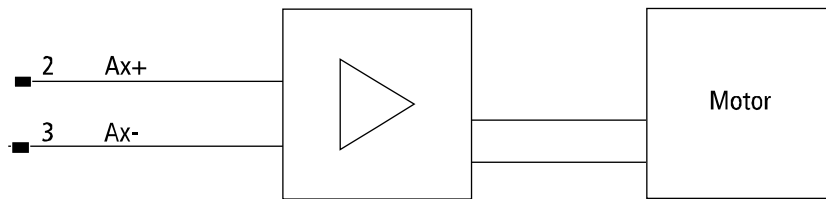
Table 1-6: Connection of the signal generators to the screw terminal panel

Signal generator			Screw terminal panel PX8001 (50-pin)							
Pin No.	Pin name	Lead colour (cable)	Signal name	Terminal name	Signal type	Terminal No.				Terminal function
						FM0	FM1	FM2	FM3	
	+24 V / U _{Ref}		+24 V / U _{Ref}	+24 V / U _{Ref}	-	34	34	34	34	see Technical Description of the board
	GND		GND	GND	-	1	1	1	1	Ground
			PWM_OUT_Ch0_x+	Ax+	RS422/TTL	2	10	18	26	PWM 0 output
			PWM_OUT_Ch0_x-	Ax-	RS422/TTL	3	11	19	27	
			PWM_OUT_Ch1_x+	Bx+	RS422/TTL	4	12	20	28	PWM 1 output
			PWM_OUT_Ch1_x-	Bx-	RS422/TTL	5	13	21	29	
			GATE_Ch0_x+	Cx+	RS422/TTL	6	14	22	30	PWM 0 gate input
			GATE_Ch0_x-	Cx-	RS422/TTL	7	15	23	31	
			GATE_Ch1_x+	Dx+	RS422/TTL	8	16	24	32	PWM 1 gate input
			GATE_Ch1_x-	Dx-	RS422/TTL	9	17	25	33	
			DIG_IN_Ex	Ex	24 V / opt. 5 V	39	40	41	42	Digital input
			DIG_IN_Fx	Fx	24 V / opt. 5 V	43	44	45	46	Digital input
			DIG_IN_Gx	Gx	24 V / opt. 5 V	47	48	49	50	Digital input
			DIG_OUT_Hx	Hx	24 V / opt. 5 V	35	36	37	38	Digital PWM 0 output or freely controllable
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-

x = Number of the function module (0-3)

1.7 Connection example

Fig. 1-4: Connection example



x = Number of the function module (0-3)

1.8 Procedure for using the PWM function

In order to use the PWM function, the following steps need to be performed:

- 1.** Select a function module.
- 2.** Select a channel.
- 3.** Select a clock signal.
- 4.** Define the Start/Stop level.
- 5.** Define the Low time.
- 6.** Define the High time.
- 7.** "i_PCl1711_InitPWM" or "i_PCl1710_InitPWM"
- 8.** Select the start condition (external gate or software start)
- 9.** Start the PWM output.

The PWM function is now ready for use.

2 Standard software

The API software functions supported by the board are listed in an HTML document. A description of how to access the respective file can be found in the document "Quick installation PC boards" (see PDF link), in the chapter "Standard software".

3 Appendix

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4 Contact and support

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